UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,104	03/06/2002	James Douglas Wehrly JR.	0254-082/D1	9757

7590 11/25/2003

J. Scott Denko
Andrews & Kurth LLP
111 Congress Avenue
Suite 1700
Austin, TX 78701

EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,104	WEHRLY, JAMES DOUGLAS	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3* is/are allowed.

6)☒ Claim(s) *6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *06 October 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings were received on October 6, 2003. These drawings are approved.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al. (USPAT 6133637, Hikita) in view of Sakai et al. (USPAT 5894984, Sakai).

Hikita discloses in figures 43 – 45 a method of creating a stack of integrated circuits selectively connected to provide increased memory density in an application. Hikita discloses in figures 43 – 45 providing a carrier frame (12) configured to have a plurality of members (12b) emergent into a window within the carrier frame. Hikita discloses in figures 43 – 45 and column 5, lines 10 – 11 applying a first portion of a solder-containing compound (14c) to the first side of the plurality of members. Hikita discloses in figures 43 – 45 placing a first packaged integrated circuit (14) having external leads (14a) extending away from the packaged integrated circuit in contact with the plurality of members. Hikita discloses in figures 43 – 45 and column 21, lines

12 – 14 processing the first integrated circuit and the carrier frame by transfer molding to create solder connections between the plurality of members and the first packaged integrated circuit. It is not clear in Hikita if the transfer molding step includes processing the combination with a heat source. Sakai teaches in figure 8a and column 1, lines 24 – 33 a transfer molding step that includes processing a combination with a heat source. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the heat source of Sakai in the transfer molding step of Hikita in order to form an encapsulating member to protect an integrated circuit device. Therefore, the combination of Hikita and Sakai teach processing the first integrated circuit and the carrier frame with a heat source to create a first set of solder connections between the plurality of members and a plurality of the external, extending away, leads of the first packaged integrated circuit. Hikita discloses in figures 43 – 45 and column 5, lines 10 – 11 applying a second portion of a solder-containing compound (16b) to the second side of the plurality of members of the carrier frame. Hikita discloses in figures 43 – 45 placing a second packaged integrated circuit (16) having external leads extending away from the second packaged integrated circuit in contact with the plurality of members. Hikita discloses in figures 43 – 45 and column 21, lines 12 – 14 processing the second integrated circuit and the carrier frame by transfer molding to create second solder connections between the plurality of members and the second integrated circuit. It is not clear in Hikita if the transfer molding step includes processing the combination with a heat source. Sakai teaches in figure 8a and column 1, lines 24 – 33 a transfer molding step that includes processing a combination with a heat source. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the heat source of Sakai in the transfer molding step of Hikita in order to form an encapsulating

member to protect an integrated circuit device. Therefore, the combination of Hikita and Sakai teach processing the second integrated circuit and the carrier frame with a heat source to create a second set of solder connections between the plurality of members and the plurality of the external, extending away, leads of the second packaged integrated circuit.

Allowable Subject Matter

4. Claims 1 – 3 are allowed.

5. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not disclose or suggest at least the claim limitations of "after said processing step, applying a second portion of a solder containing compound to the second side of the plurality of members of the carrier frame; after applying the second portion of solder-containing compound, placing a second packaged integrated circuit in contact with the plurality of members".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703) 308-6236. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
November 24, 2003